



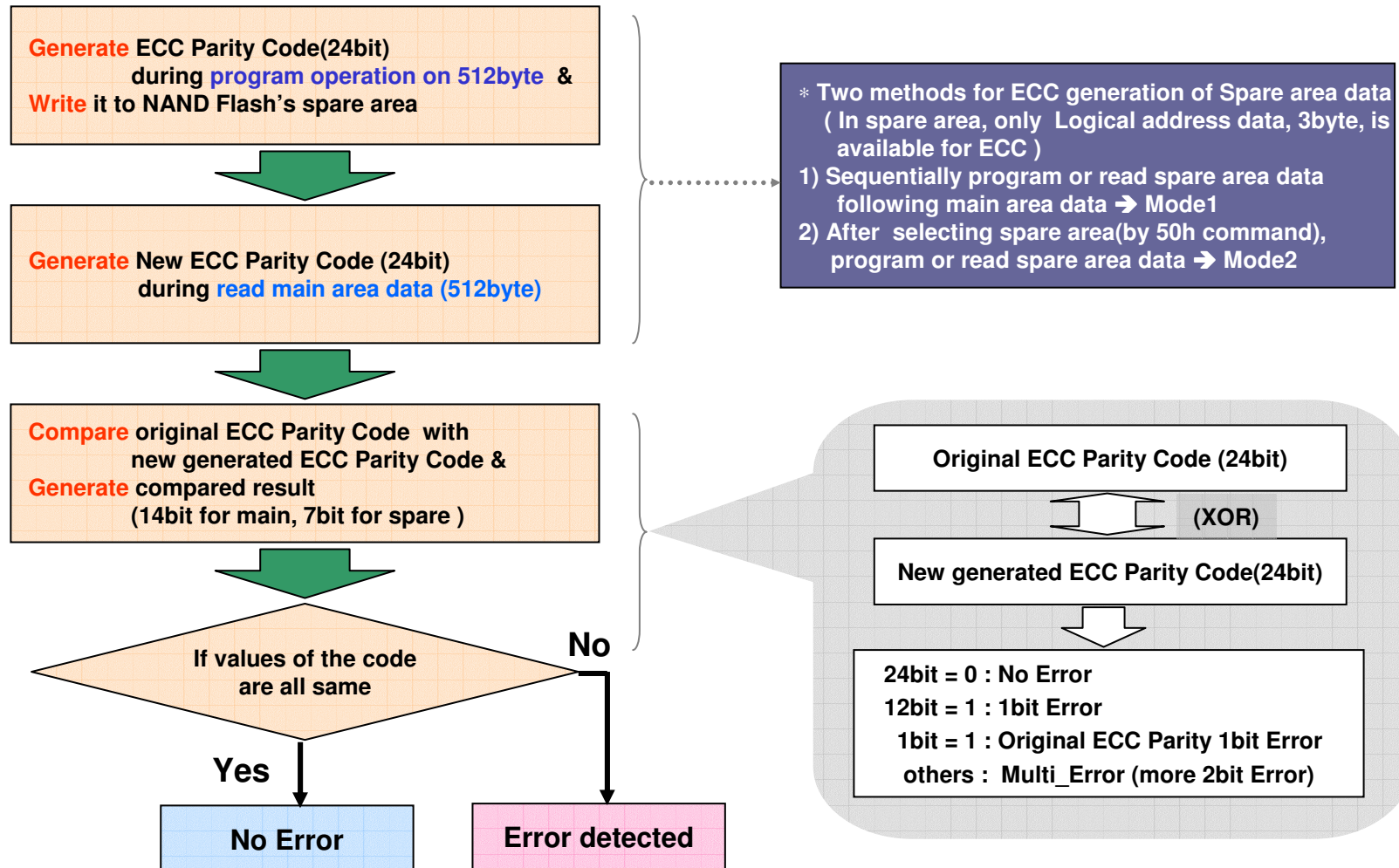
ECC Algorithm (512Byte)

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**This is only example algorithm for SW ECC.
In case of OneNAND which supports HW ECC, parity bit position can be changed.**

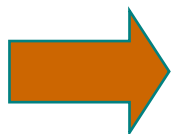
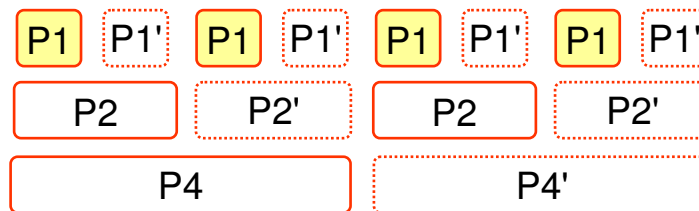
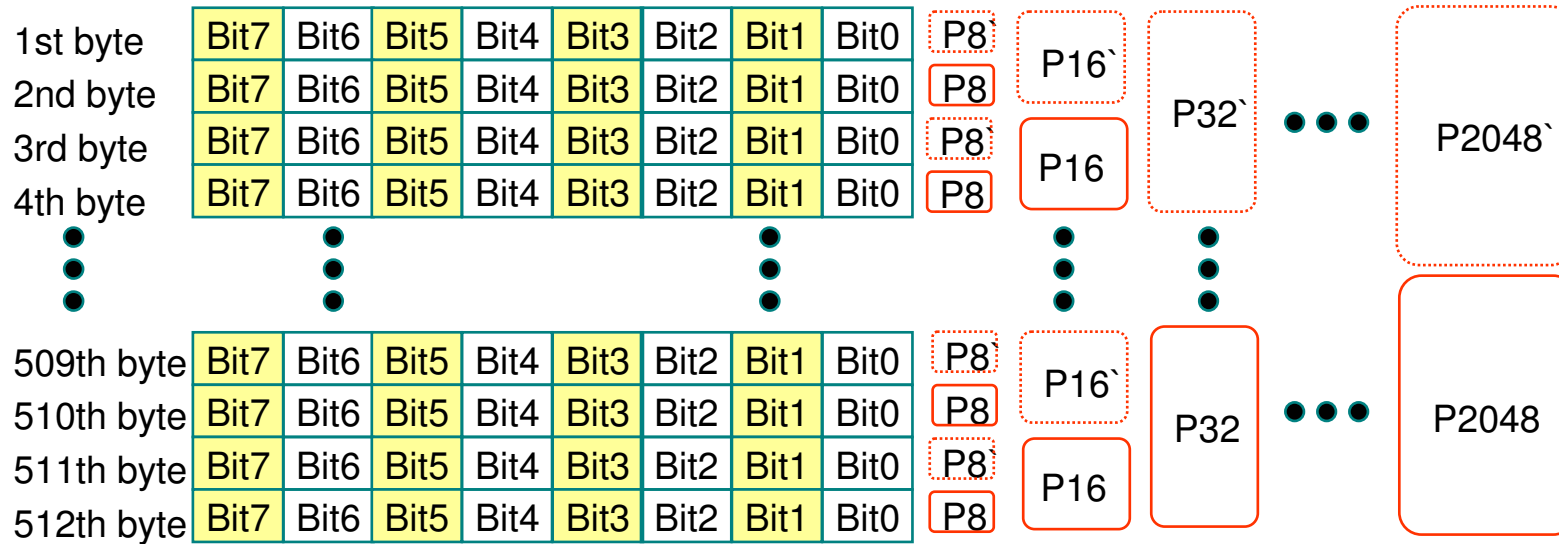
Processing Procedure

For 512Byte



Parity Generation for Main Array (Column)

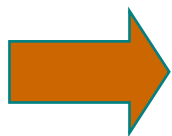
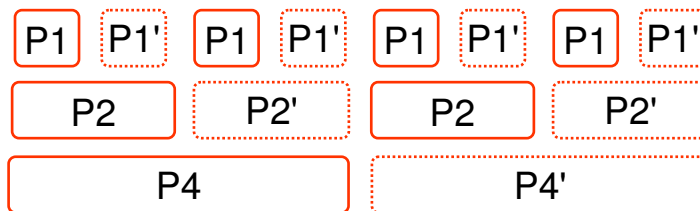
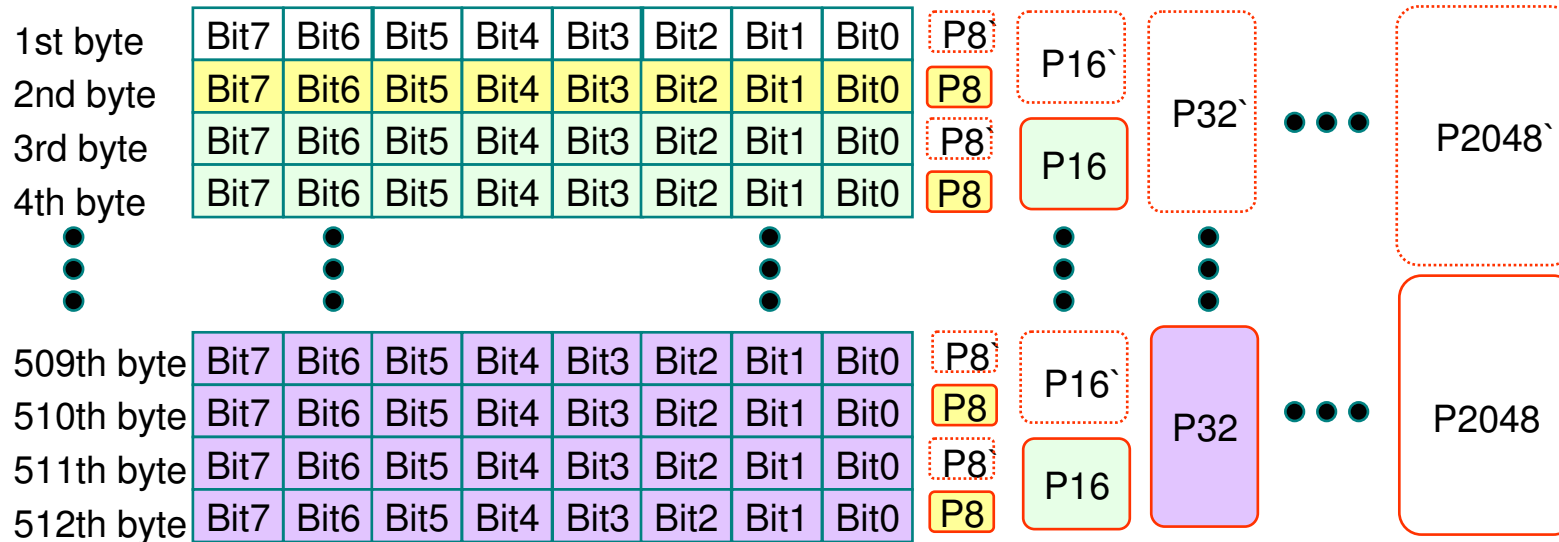
For 512Byte



$$\begin{aligned}
 P1 &= \text{bit7} \oplus \text{bit5} \oplus \text{bit3} \oplus \text{bit1} \oplus P1 \\
 P2 &= \text{bit7} \oplus \text{bit6} \oplus \text{bit3} \oplus \text{bit2} \oplus P2 \\
 P4 &= \text{bit7} \oplus \text{bit6} \oplus \text{bit5} \oplus \text{bit4} \oplus P4
 \end{aligned}$$

Parity Generation for Main Array (Row)

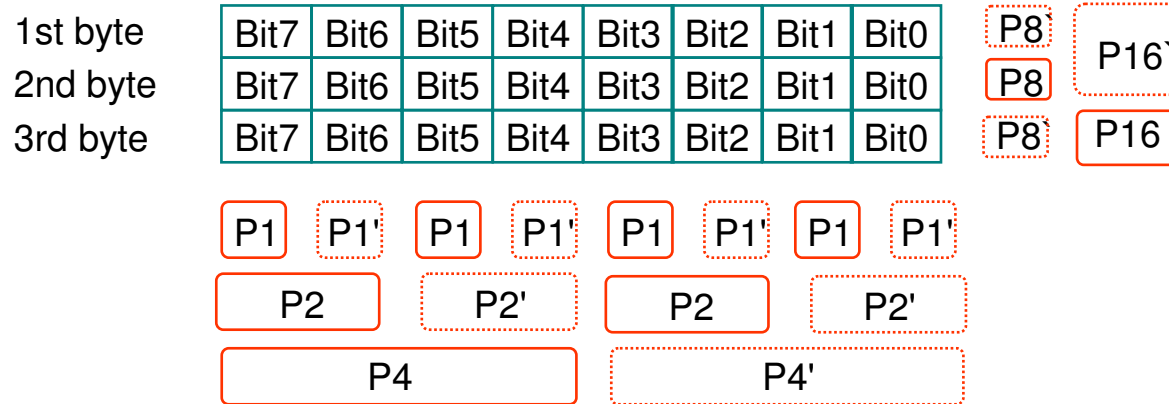
For 512Byte



$$P8 = \text{bit7} \oplus \text{bit6} \oplus \text{bit5} \oplus \text{bit4} \oplus \text{bit3} \oplus \text{bit2} \oplus \text{bit1} \oplus \text{bit0} \oplus P8$$

Parity Generation for Spare Array (Logical Address)

For 512Byte



➔

$$\begin{aligned}
 P1_s &= \text{bit7} \oplus \text{bit5} \oplus \text{bit3} \oplus \text{bit1} \oplus P1 \\
 P2_s &= \text{bit7} \oplus \text{bit6} \oplus \text{bit3} \oplus \text{bit2} \oplus P2 \\
 P4_s &= \text{bit7} \oplus \text{bit6} \oplus \text{bit5} \oplus \text{bit4} \oplus P4 \\
 P8_s &= \text{bit7} \oplus \text{bit6} \oplus \text{bit5} \oplus \text{bit4} \oplus \text{bit3} \oplus \text{bit2} \oplus \text{bit1} \oplus \text{bit0} \oplus P8 \\
 &\vdots
 \end{aligned}$$

ECC CODE FORMAT STANDARD

For 512Byte

■ X8 org. NAND Flash

● ECC Code for Main area data

P1~P4 : Column Parity , P8~P2048 : Row Parity

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC0	~P64	~P64'	~P32	~P32'	~P16	~P16'	~P8	~P8'
ECC1	~P1024	~P1024'	~P512	~P512'	~P256	~P256'	~P128	~P128'
ECC2	~P4	~P4'	~P2	~P2'	~P1	~P1'	~P2048	~P2048'

● ECC Code for LSN data

P1_s : Column Parity , P2_s~P16_s : Row Parity

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
S_ECC0	~P2_s	~P2'_s	~P1_s	~P1'_s	~P16_s	~P16'_s	~P8_s	~P8'_s
S_ECC1	1	1	1	1	1	1	~P4_s	~P4'_s

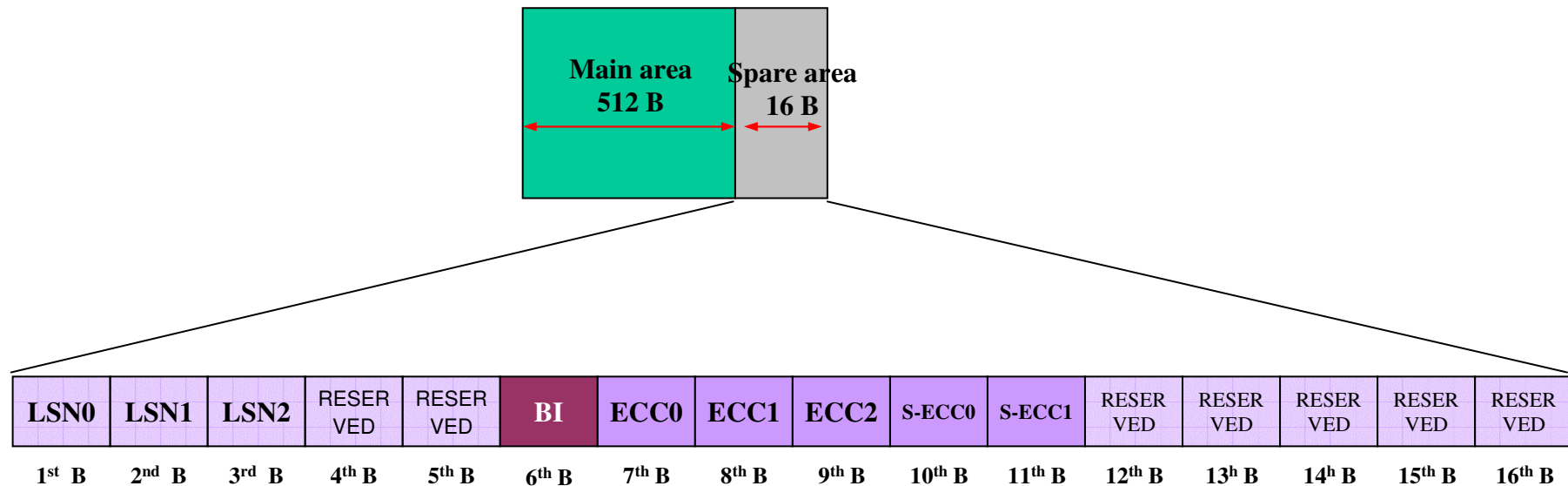
* ~ : Logically Inverse operation

SPARE AREA ASSIGNMENT STANDARD

For 512Byte

■ Small Page(528B) & X8 org. NAND Flash

- Device : 64Mb, 128Mb, 256Mb, 512Mb, 1Gb DDP



- > LSN : Logical Sector Number
- > ECC0,ECC1,ECC2 : ECC code for Main area data
- > S_ECC0,S_ECC1 : ECC code for LSN data
- > BI : Bad block Information

Compare Result Table

For 512Byte

- For Main Array 512byte

Stored ECC(in Spare area) [P2048P2048'P1024P1024'...P2P2'P1P1']

⊕ Computed data's ECC result [P2048P2048'P1024P1024'...P2P2'P1P1']

	No Error	1bit Error	ECC Parity 1bit Error	Multi_Error
XORed Results	24 bits : 0	12 bits : 1	1 bit : 1	Others

error position is
P2048P1024P512...P4P2P1

- For Spare Array 3byte

Stored ECC(in Spare area) [P16P16'P8P8'P4P4'P2P2'P1P1']

⊕ Computed LSN's ECC result [P16P16'P8P8'P4P4'P2P2'P1P1']

	No Error	1bit Error	ECC Parity 1bit Error	Multi_Error
XORed Results	10 bits : 0	5 bits : 1	1 bit : 1	Others

error position is
P16P8P4P2P1